RF and Microwave Frequency Properties of a Reverse-Biased Thick Switching p-i-n Diode

Lioudmila Drozdovskaia

***Abstract*—The frequency response of the dc reverse-bias voltage keeping high-impedance p-i-n diode in low-distortion state is studied using different mathematical and theoretical models. This paper discusses the comparison between the theoretical and experimental results.**

***Index Terms*—p-i-n diode, reverse bias voltage, switch.**

I. Introduction

THERE IS strong interest in high-power RF and microwave semiconductor control devices. They are very attractive for different applications in various modern systems such as high-power radar, wireless power transmission, etc. [1]. p-i-n diodes were successfully used in various controls devices about 40 years [2], [3]. They still remain the main solid-state components of high-power microwave and RF control devices. Silicon and gallium–arsenide p-i-n diodes are preferred over other semiconductor components (transistors, Schottky barrier diodes, etc.) due to their higher power-handling capability.

A large-signal environment may cause unwanted detection effects in p-i-n diodes. To eliminate these effects, dc reverse-bias voltage is used. The correct determination of this voltage is very important for RF and microwave control devices design. There are a limited number of publications devoted to this problem (e.g., [4] and [7]).

This paper presents computer simulation results of the reverse-biased thick silicon p-i-n diode in RF and microwave high-power mode. The required dc-bias voltage determined by using different mathematical and physical models of p-i-n diodes is compared with the experimental results.

II. p-i-n Diode Switch

A simple shunt-type p-i-n diode switch is under consideration. Its circuit is shown in Fig. 1. The p-i-n diode shunts the transmissions line with the characteristic impedance Z_c and matched load. The dc part of the switch is isolated from the microwave part by the decoupling choke $L_{\rm dec}$. An impulse generator provides the forward-biasing current for the diode. The p-i-n-diode is in a low-impedance state in this case and the main part of the input microwave power $P_{\rm in}$ is reflected and a good isolation is achieved. The other state of the diode is realized with the dc reverse-bias voltage U_o. In this case, the p-i-n diode is in a high-impedance state. It provides low insertion loss and the output power $P_{\rm out}$ only slightly differs from the input power. The dc reverse-bias voltage reduces the harmonic distortion in the p-i-n diode and decreases the switch insertion loss.

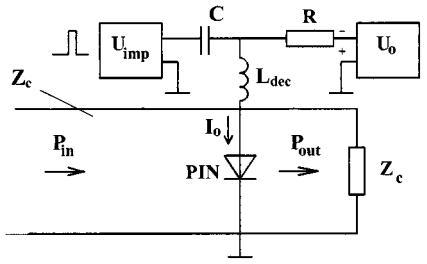

Fig. 1. p-i-n diode switch circuit.

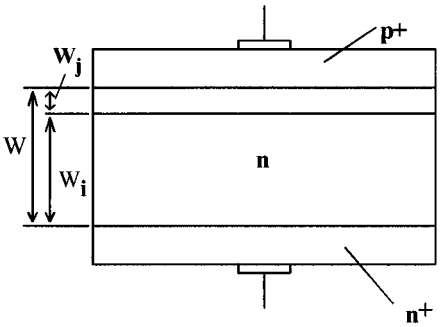

Fig. 2. Model of the thick p-i-n-diode.

III. Computer Simulation Models

A. Impedance Model

The first model used in this paper for computer simulation was the impedance multilayer model of a p-i-n diode [7]–[10]. This model considers the I-region of the diode below punchthrough consisting of undepleted and depleted regions (Fig. 2). The p-i-n diode equivalent circuit is presented in Fig. 3. The depleted region width W_j and capacitance C_j of a reverse-biased p-i-n diode can be found using the following equations:

$$W_j = W_{j0} \times \sqrt{1 + \frac{U_o}{U_k}} \tag{1}$$

$$C_j = \frac{C_{jo}}{\sqrt{1 + \frac{U_o}{U_k}}} \tag{2}$$

$$W_{jo} = \sqrt{\frac{2\varepsilon_i U_k}{eN}} \tag{3}$$

$$C_{j0} = \frac{\varepsilon_i S}{W_{jo}} \tag{4}$$

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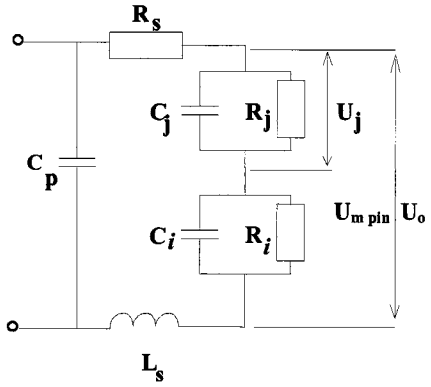

Fig. 3. p-i-n-diode equivalent circuit.

where W_{j0} is the depleted region width of the unbiased diode, C_{jo} is the depleted region capacitance in the unbiased state, U_k is the built-in potential, U_0 is the dc reverse-bias voltage, e is the single charge, N is the I-layer doping level, and ε_i is the silicon dielectric permittivity. The depleted region resistance R_j was assumed to be about the order of several megaohms.

The undepleted region capacitance C_i and resistance R_i are

$$C_i = \frac{\varepsilon_i S}{W - W_j} \tag{5}$$

$$R_i = \frac{1}{e\mu N} \times \frac{W - W_j}{S} \tag{6}$$

where the W is the I-layer width and μ is the carrier mobility.

Parasitic bond-wire inductance L_s, ohmic contacts or passive regions resistance R_s, and package parasitic capacitance C_p (in the case of packaged p-i-n diodes) are also admitted in this equivalent circuit.

The transit time effect leads to the reduction of the voltage across the depleted region U_j in $1/F(\theta_j)$ times. The empirical function of the nonzero carrier transit time through depleted region $F(\theta_j)$ depends on the diode geometry, semiconductor material properties, RF or microwave input power, and applied dc reverse-bias voltage [10].

When the diode is unbiased or reverse-biased, depleted region resistance R_j is much higher than the resistance of undepleted region R_i.. Thus, the dc reverse-bias voltage is applied mainly to the depleted region (to the p^+–n junction). Depleted and undepleted regions form the frequency-dependent impedance divider. Applied ac voltage is divided between two regions in the I-layer according to its frequency properties. In this model, it was proposed that the p^+–n junction begins to generate harmonic distortions above the minimal permissible level when the overall voltage across the depleted region exceeds the threshold voltage $U_{t\,\mathrm{eff}}$, which is about 0.1-0.2 V [7].

This condition leads to the expression for the required reverse-bias dc voltage $U_{0\,\min}$ (for $L_s \approx 0$ and $R_s \approx 0$) as [7]

$$U_{0\,\min} = U_{m\mathrm{pin}} \times F(\Theta_j)\left|1 + \frac{R_i}{R_j} \times \frac{1 + j2\pi f C_j R_j}{1 + j2\pi f C_i R_i}\right|^{-1} - U_{t\,\mathrm{eff}} \tag{7}$$

where f is the operating frequency and $U_{m\mathrm{pin}}$ is the RF or microwave amplitude across the diode. Considering (1) and (2), one can see that (7) is the nonlinear equation with $U_{0\,\min}$: $U_{0\,\min} = \Phi(U_{0\,\min})$ and it requires to be solved iteratively.

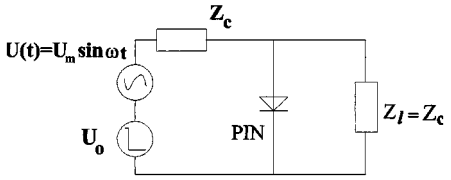

Fig. 4. p-i-n-diode analysis circuit.

B. One-Dimensional Drift–Diffusion Model

A computer program [11] based on the one-dimensional isothermal drift–diffusion model of a semiconductor component has been used for computer simulation. Fig. 4 shows the circuit configuration used in these simulations. The load resistance Z_l and series resistance Z_C are equal to the transmission-line characteristic impedance of 50 Ω.

Input data to the program is the geometry of the semiconductor and contact regions, the doping profile of the p-i-n diode, and the values of lumped elements forming the circuit. The program numerically solves the continuity equations for electrons and holes, the Poisson equation, and the total current equation. To approximate the steady-state operation of the diode, several tens of the input ac-signal cycles have been used. The waveforms of diode voltage and current are computed with an input signal $V(t)$ at fixed frequency and amplitude and fixed value of the dc reverse-bias voltage. The nonlinear distortion factor K_{dist} was evaluated from this data using a Fourier analysis program. The value of the nonlinear distortion factor was determined as

$$K_{\mathrm{dist}} = \frac{\sum_{i=2}^{10} U_i^2}{U_1^2} \tag{8}$$

where U_1 is the first harmonic amplitude and $U_2, \ldots, U_{10}$ are the higher harmonics amplitudes.

The nonlinear distortion factor K_{dist} of 10^{-4} has been chosen as the minimal permissible level of harmonic distortions. The threshold voltage $U_{t\,\mathrm{eff}}$ of 0.1-0.2 V in the impedance model and the distortion factor K_{dist} of 10^{-4} in the drift–diffusion model both provide the dc current generated by the p-i-n diode in the order of several microamperes.

The third model used in simulations were based on the expressions of [6], which were based on I-region electron and holes transit-time effects.

IV. Computer Simulation Results

Computer simulation using different models was performed in a wide range of frequencies and RF amplitudes for the silicon p-i-n diode with a p^+–n–n^+ structure. The 150-μm diode had been used in simulation. It had a cross section of 3.14×10^{-2} cm^2, an I-layer doping level of 5×10^{12} cm^{-3}, and electron and hole lifetimes of 10^{-5} s. The diode doping profile was assumed to be abrupt with acceptor p^+ and donor n^+ concentrations of 5×10^{19} cm^{-3} and 10^{20} cm^{-3}, respectively.

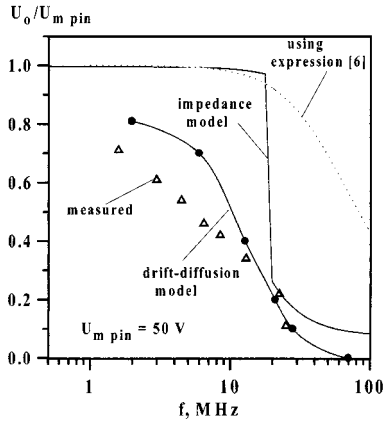

Fig. 5. Theoretical and experimental results for the 150-μm p-i-n diode [12].

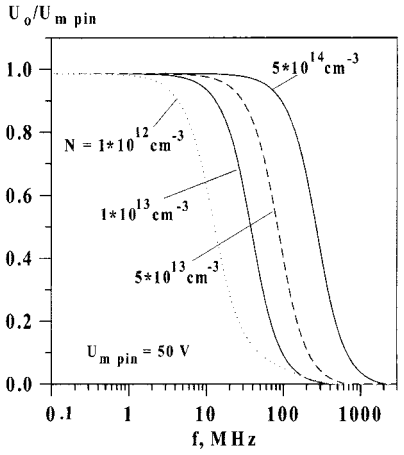

Fig. 6. Theoretical minimal reverse bias voltage versus frequency for the 450-μm Si p-i-n diode with different I-layer doping levels.

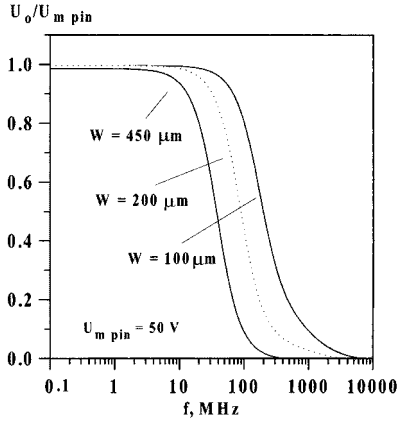

Fig. 7. Theoretical minimal reverse bias voltage versus frequency for the p-i-n diodes with a different I-layer width and I-layer doping level of 1×10^{13} cm^{-3}.

Fig. 5 shows the measured [12] and computed minimum required reverse-bias dc voltage U_0 using three different models. All models provide a quite good general agreement between the models and experimental results, also shown in this figure. Model [6] takes into account only the transit time effects and it overestimates the required reverse-bias voltage in a considerable frequency range.

The impedance model in addition to the transit time effect considers the field distribution inside the I-layer between the depleted and undepleted regions. Most of the reverse dc bias voltage applied to the p-i-n diode always drops across the depleted region (near the p^+–n junction), while the ac input signal is divided between the depleted and undepleted regions according to the properties of the frequency-dependent divider. The impedances of depleted region Z_j and undepleted region Z_i form this divider.

To prevent any unwanted detection effects, the dc reverse-bias voltage across the depleted region should be at least equal to the amplitude of the ac voltage across it. At low frequencies, $Z_i \approx R_i$ and $Z_j \approx R_j$. Taking into account the fact that $R_j \gg R_i$, the distribution of ac voltage across the diode is similar with the dc voltage distribution. Thus, to avoid any detection effects at low frequencies, it is necessary to apply the dc reverse-bias voltage of $U_{0\min} \approx U_{m\mathrm{pin}}$.

In very high frequencies, $Z_i \approx 1/\omega C_i$ and $Z_j \approx 1/\omega C_j$. For the thick p-i-n diode, $W_j \ll W$, therefore, $C_j \gg C_i$. In this case, most of the ac voltage is dropped across the undepleted region. Thus, to prevent any detection effects, it is possible to apply dc reverse-bias voltage $U_{0\min} \ll U_{m\mathrm{pin}}$. The transition effect is highly pronounce only in the high-frequency area , and it leads to an additional decrease of the ac voltage across the depleted region. Finally, with the further frequency increase, this effect provides the full absence of any detection effects in the p-i-n diode. Equation (7) reflects all these situations.

The more exact results are provided by a one-dimensional isothermal drift–diffusion model of the semiconductor device (see Fig. 5). This model includes a wide range of effects in the semiconductor, such as: 1) avalanche breakdown and nonlinear phenomena connected with high doping and high-level injection and 2) carrier lifetime lowering and bandgap narrowing in emitter regions, Auger recombination, and electron-hole scattering. On the other hand, it leads to a problem with computational time. For the fast prediction of the required reverse-bias voltage, the impedance model is preferable because it allows a fast computation with enough accuracy.

An impedance model was implemented to find the reverse-bias-mode parameters (input ac voltage, operating frequency, required dc reverse-bias voltage) relation with the p-i-n diode geometry and diode semiconductor material properties [7]. Fig. 6 shows the frequency response of the required minimal dc-bias reverse voltage applied to the 450-μm Si p-i-n diode versus the I-layer doping level. The ac voltage of 50 V was applied across the diode. Fig. 7 reflects the frequency response of the required minimal dc-bias reverse voltage applied to the Si p-i-n diode with the I-layer doping level of 1×10^{13} cm^{-3} versus the I-layer width with the same applied ac voltage.

In both figures, one can see a sharp change in the frequency response of the required reverse-bias voltage. The minimal required dc reverse-bias voltage drastically decreases with the frequency increase. Properties of the above-mentioned impedance divider cause the decrease of the ac voltage dropped across the depleted region with an increase in frequency. Thus, the required minimal dc reverse-bias voltage might also be decreased. The frequency region of this decreasing depends on the different diode and regime parameters, as illustrated in Figs. 6 and 7. These results are in accordance with previous experimental data [12].

V. Conclusion

In this paper, the impedance model has been used to analyze a reverse-bias mode of a thick silicon p-i-n diode. This model is a convenient approximation, taking into account two different areas inside the I-layer. It has been verified both experimentally and theoretically using a one-dimensional drift–diffusion model. Some of the important properties of thick p-i-n diodes under reverse-bias voltage have been estimated. The next step may contain computer simulation development based on a two-dimensional drift–diffusion model [13].

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